CLAIMS

What is Claimed is:

1. A method of determining a gate oxide thickness of an operational MOSFET (metal oxide semiconductor field effect transistor) fabricated with a gate oxide formation process, comprising:

a) providing said operational MOSFET fabricated with said gate oxide formation process;

b) coupling a drain node and a source node of said operational MOSFET to a ground;

c) applying a range of voltages at a gate node of said operational MOSFET and measuring at said gate node a gate direct tunneling current for each applied voltage to generate a plurality of measured data;

d) providing a gate direct tunneling current model; and

e) determining said gate oxide thickness by fitting said gate direct tunneling current model to said measured data and using a gate oxide thickness variable as a fitting parameter.

2. A method as recited in Claim 1 wherein said gate oxide thickness is no less than approximately 3 nanometers.

3. A method as recited in Claim 1 wherein said gate oxide thickness is no greater than approximately 3 nanometers.

4. A method as recited in Claim 1 wherein a channel length of said operational MOSFET is no less than approximately 0.5 micrometers.

5. A method as recited in Claim 1 wherein a channel length of said operational MOSFET is no greater than approximately 0.5 micrometers.

6. A method as recited in Claim 1 wherein a channel width of said operational MOSFET is no less than approximately 5 micrometers.

7. A method as recited in Claim 1 wherein a channel width of said operational MOSFET is no greater than approximately 5 micrometers.

8. A method as recited in Claim 1 wherein in said step c) said operational MOSFET is operated in an inversion mode by application of a particular range of voltages at said gate node.

9. A method as recited in Claim 1 wherein said gate direct tunneling current model includes a value representing reflectivity of an electron from an inversion layer due to a gate oxide energy barrier.

10. A method of determining a gate oxide thickness of an operational NMOSFET (n-type metal oxide semiconductor field effect transistor), comprising:

a) coupling a drain node and a source node of said operational NMOSFET to a ground;

b) applying a range of voltages at a gate node of said operational NMOSFET and measuring at said gate node a gate direct tunneling current for each applied voltage to generate a plurality of measured data;

c) providing a gate direct tunneling current model; and

d) determining said gate oxide thickness by fitting said gate direct tunneling current model to said measured data and using a gate oxide thickness variable as a fitting parameter.

11. A method as recited in Claim 10 wherein said gate oxide thickness is no less than approximately 3 nanometers.

12. A method as recited in Claim 10 wherein said gate oxide thickness is no greater than approximately 3 nanometers.

13. A method as recited in Claim 10 wherein a channel length of said operational NMOSFET is no less than approximately 0.5 micrometers.

14. A method as recited in Claim 10 wherein a channel length of said operational NMOSFET is no greater than approximately 0.5 micrometers.

15. A method as recited in Claim 10 wherein a channel width of said operational NMOSFET is no less than approximately 5 micrometers.

16. A method as recited in Claim 10 wherein a channel width of said operational NMOSFET is no greater than approximately 5 micrometers.

17. A method as recited in Claim 10 wherein in said step b) said operational NMOSFET is operated in an inversion mode by application of a particular range of voltages at said gate node.

18. A method as recited in Claim 10 wherein said gate direct tunneling current model includes a value representing reflectivity of an electron from an inversion layer due to a gate oxide energy barrier.

19. A system for determining a gate oxide thickness, comprising:

an operational MOSFET (metal oxide semiconductor field effect transistor) fabricated with a gate oxide formation process, said operational MOSFET including a drain node coupled to a ground, a source node coupled to said ground, and a gate node, wherein a range of voltages are applied at said gate node and a gate direct tunneling current is measured at said gate node for each applied voltage to generate a plurality of measured data; and

a data processor for determining said gate oxide thickness by fitting a gate direct tunneling current model to said measured data and using a gate oxide thickness variable as a fitting parameter.

20. A system as recited in Claim 19 wherein said gate oxide thickness is no less than approximately 3 nanometers.

21. A system as recited in Claim 19 wherein said gate oxide thickness is no greater than approximately 3 nanometers.

22. A system as recited in Claim 19 wherein a channel length of said operational MOSFET is no less than approximately 0.5 micrometers.

23. A system as recited in Claim 19 wherein a channel length of said operational MOSFET is no greater than approximately 0.5 micrometers.

24. A system as recited in Claim 19 wherein a channel width of said operational MOSFET is no less than approximately 5 micrometers.

25. A system as recited in Claim 19 wherein a channel width of said operational MOSFET is no greater than approximately 5 micrometers.

26. A system as recited in Claim 19 wherein said operational MOSFET is operated in an inversion mode by application of a particular range of voltages at said gate node.

27. A system as recited in Claim 19 wherein said gate direct tunneling current model includes a value representing reflectivity of an electron from an inversion layer due to a gate oxide energy barrier.